

WHAT IS CLAIMED IS:

1. A data driving apparatus for a liquid crystal display device, comprising:

a first multiplexer part performing a time-division on inputted digital pixel data;

a digital-analog converter part converting the time-divided digital pixel data from the first multiplexer part to analog pixel signals;

a demultiplexer part supplying the analog pixel signals from the digital-analog converter part to a plurality of output channels; and

an output part sampling and holding first received analog pixel signals from the demultiplexer part and holding second received analog pixel signals and simultaneously outputting both first and second received pixel signals to corresponding data lines.

2. The apparatus according to claim 1, wherein the digital-analog converter part coupled to the output channels of the demultiplexer part.

3. The apparatus according to claim 1, wherein the digital-analog converter part comprises:

a positive digital-analog converter converting the digital pixel data to a positive pixel signal;

a negative digital-analog converter converting the digital pixel data to a negative pixel signal; and

a second multiplexer part selecting one of the positive and the negative pixel signals in accordance with a polarity control signal and providing the selected pixel signal with the demultiplexer part.

4. The apparatus according to claim 1, wherein the output part comprises:

a sampling part sampling the pixel signals from odd-numbered or even-numbered output channels of the demultiplexer part;

a capacitor part receiving and holding the sampled pixel signals from the output channels of the demultiplexer part;

an output buffer part coupled to the capacitor part; and

a third multiplexer part simultaneously discharging the pixel signals held in the capacitors to the corresponding data lines through the output buffer part.

5. The apparatus according to claim 4, further comprising:

a shift register sequentially shifting an input source start pulse in accordance with an input source shift clock to generate a sampling signal; and

a latch part sequentially latching the pixel data in response to the sampling signal and simultaneously providing the latched pixel data to the first multiplexer during an enable period of an input source output enable signal.

6. The apparatus according to claim 5, wherein the second multiplexer provides the corresponding data lines with the pixel signals held in the capacitors for the enable period of the source output enable signal and a reference voltage of liquid crystal cells for the disabled period of the source output enable signal.

7. The apparatus according to claim 1, wherein the first multiplexer and the demultiplexer part are controlled by an ODD/EVEN signal which performs the time-division for a horizontal period.

8. The apparatus according to claim 4, wherein the sampling switches controlled by an ODD/EVEN signal which performs the time-division on a horizontal period.

9. A data driving apparatus for a liquid crystal display device, comprising:

a multiplexer part performing a time-division on inputted digital pixel data and providing the time-divided pixel data through output channels having a selected polarity;

a digital-analog converter part converting the time-divided digital pixel data from the multiplexer into analog pixel signals with the selected polarity;

a demultiplexer part providing the time-divided pixel signal from the digital-analog converter to different output channels with the selected polarity; and

an output part sampling and holding the time-divided pixel signals from the demultiplexer through a path with the selected polarity and outputting the pixel signals to corresponding data lines for a next horizontal period.

10. The apparatus according to claim 9, wherein the digital-analog converter part comprises:

a positive digital-analog converter converting the pixel signals provided through positive output channels of the multiplexer into positive pixel signals; and

a negative digital-analog converter converting the pixel signals provided through negative output channels of the multiplexer into negative pixel signals.

11. The apparatus according to claim 9, wherein the multiplexer part comprises:

a plurality of positive path switches coupled to input channels for the pixel data and commonly connected to positive output channels; and

a plurality of negative path switches coupled to the input channels for the pixel data in parallel, connected to the positive path switches in parallel, and commonly connected to negative output channel.

12. The apparatus according to claim 9, wherein the demultiplexer part comprises:

a plurality of positive path switches forming a plurality of different positive paths, and commonly connected to a positive digital-analog converter, wherein the positive path switches connected to output channels of the positive digital-analog converter; and

a plurality of negative path switches forming a plurality of different negative paths, commonly connected to a negative digital-analog converter, wherein the negative path switches are connected to the positive path switches in parallel and connected to the positive channel switches of the output channels of the negative digital-analog converter.

13. The apparatus according to claim 9, wherein the output part comprises:

a sampling part sampling the pixel signal supplied through the output channels of the demultiplexer and providing the sampled pixel signal to corresponding paths having a different polarity from each other;

a holding part holding the pixel signals provided through the corresponding paths of the sampling part; and

a discharging part discharging the pixel signals held in the holding part for a first period to the corresponding data lines through the different polarity paths for a second period.

14. The apparatus according to claim 13, wherein the sampling part and the holding part sample and hold the pixel signals supplied for the second period through the channel different from that of the pixel signal supplied for the first period.

15. The apparatus according to claim 13, wherein the sampling part has a second demultiplexer part comprising;

a plurality of the positive path switches forming a plurality of different positive paths and connected to the output channels of the demultiplexer part; and

a plurality of negative path switches connected to the output channels of the demultiplexer, and connected to the positive path switches in parallel.

16. The apparatus according to claim 15, wherein the holding part comprises:

a positive path capacitor charging and holding the positive pixel signals from the positive path switches of the second demultiplexer part; and

a negative path capacitor charging and holding the negative pixel signals from the negative path switches of the second demultiplexer part.

17. The apparatus according to claim 15, wherein the discharging part comprises:

a plurality of positive path switches connected to the positive path switches of the second demultiplexer through the holding part and connected to the data lines; and

a second demultiplexer part having the negative path switches connected to the negative switches of the second demultiplexer through the holding part and connected to the negative channel switches and the data lines in parallel.

18. The apparatus according to claim 17, wherein the multiplexer, the demultiplexer, and the second demultiplexer are controlled by a first control signal through an input polarity control signal and an ODD/EVEN signal performing the time-division on a horizontal period.

19. The apparatus according to claim 18, wherein the ODD/EVEN signal performs the time-division on an enable period

determined by a source output enable signal for the horizontal period.

20. The apparatus according to claim 18, wherein the ODD/EVEN signal further performs the time-division on a disable period of the source output enable signal.

21. The apparatus according to claim 20, wherein the multiplexer part, the demultiplexer part, and the second demultiplexer part recharge the holding part with the pixel signals for the disable period, wherein the pixel signals are generated for a previous enable period.

22. The apparatus according to claim 21, wherein the source output enable signal is generated by increasing the disable period of an external reference source output enable signal in order to secure a recharging period of the holding part.

23. The apparatus according to claim 18, the second multiplexer part is controlled by the first control signal and

a second control signal that is phase-inversed with respect to the first control signal.

24. The apparatus according to claim 18, further comprising an output buffer part buffering the pixel signal discharged from the holding part to the discharging part.

25. The apparatus according to claim 24, wherein the output buffer part comprises:

a plurality of positive path output buffers connected between the positive path capacitors of the holding part and the positive path switches of the second multiplexer part; and

a plurality of negative path output buffers connected between the negative path capacitors of the holding part and the negative path switches of the second multiplexer part.

26. The apparatus according to claim 17, further comprising an output buffer part buffering the pixel signal supplied through the output channels of the second multiplexer part and supplying the pixel signals to each of the data lines.

27. The apparatus according to claim 26, the output buffer part comprises:

a plurality of output buffers connected between the output channels of the second multiplexer part and the data lines.

28. The apparatus according to claim 9, further comprising:

a shift register sequentially shifting an input source start pulse in accordance with an input source shift clock to generate a sampling signal;

a latch part latching pixel data and simultaneously providing the multiplexer part with the latched pixel data for the enable period of the input source output enable signal; and

a level shifter part raising a voltage of the pixel data from the multiplexer part to supply the pixel data to the digital-analog convert part.

29. The apparatus according to claim 17, further comprising a third multiplexer part supplying the pixel signals from the output part to the corresponding data lines

for the enable period of the source output enable signal and commonly supplying a reference voltage of the liquid crystal cells to the corresponding data lines for the disable period of the source output enable signal.

30. A data driving method for a liquid crystal display device, comprising:

performing a time-division on a digital pixel data;

converting the time-divided digital pixel data into time-divided analog pixel signals;

supplying the time-divided analog pixel signals to corresponding output channels; and

sampling and holding first inputted pixel signals through a first part of the output channels and holding second inputted pixel signals from a second part of the output channels, and simultaneously supplying the first and second held pixel signals corresponding data lines.

31. The method according to claim 30, wherein the first and second held pixel signals are supplied to the corresponding data lines for an enable period of an input source output enable signal and a reference voltage of liquid

crystal cells is commonly supplied to the corresponding data lines for a disable period.

32. The method according to claim 30, wherein the converting the time-divided digital pixel data comprises:

converting the time-divided pixel data to a positive analog pixel signal and a negative analog pixel signal; and

selecting one of the positive and the negative analog pixel signals in accordance with a polarity control signal.

33. The method according to claim 30, further comprising buffering the held pixel signals through an output buffer part prior to supplying the held pixel signals to the corresponding data lines, wherein the output buffer part is connected to the corresponding data lines.

34. The method according to claim 30, wherein the sampling the pixel signals is controlled by an ODD/EVEN signal performing a time-division on a horizontal period.

35. A data driving method for a liquid crystal display device, comprising:

performing a time-division on a digital pixel data and providing the time-divided digital pixel data through output channels having a selected polarity;

converting the time-divided digital pixel data into analog pixel signals having the selected polarity;

sampling and holding the time-divided analog pixel signals to output channels having the selected polarity; and

outputting the held pixel signals to corresponding data lines for a next horizontal period.

36. The method according to claim 35, wherein the performing a time-division on a digital pixel data and the converting the time-divided digital pixel data are controlled by an input polarity control signal and a first control signal through an ODD/EVEN signal performing a time-division on a horizontal period.

37. The method according to claim 36, wherein the ODD/EVEN signal performs a time-division on an enable period determined by a source output enable signal.

38. The method according to claim 36, wherein the ODD/EVEN signal performs a time-division on a disable signal of a source output enable signal.

39. The method according to claim 38, wherein the pixel signals are sampled and held by the ODD/EVEN signal for the disable period, wherein the pixel signals in a present enable period are the same as the pixel signals in a previous enable period.

40. The method according to claim 39, wherein the disable period of the source output enable signal is determined by increasing the disable period of a reference source output enable signal inputted from an external source.

41. The method according to claim 35, wherein the outputting the held pixel signals is controlled by a first control signal and a second control signal having a phase inversion with respect to the first signal.

42. The method according to claim 35, wherein the performing a time-division on a digital pixel data is carried

out by outputting the time-divided pixel data with a polarity through the time-divided pixel data of the output channel opposite to that of the time-divided pixel data for a previous period and an adjacent channel.

43. The method according to claim 35, wherein the performing a time-division on a digital pixel data is carried out by converting the time-divided pixel data into the time-divided pixel data with a polarity opposite to that of the time-divided analog signal of a previous period and an adjacent channel.

44. The method according to claim 35, wherein the sampling and holding the time-divided analog pixel signals is performed by sampling and holding the time-divided pixel signal through a path with a polarity opposite to that of time-divided pixel signal of a previous period and an adjacent channel.

45. The method according to claim 35, wherein the output held pixel signals is buffered through an output buffer part prior to supplying to the corresponding data lines, wherein

the output buffer part is connected to the corresponding data lines.

46. The method according to claim 35, wherein the held pixel signals are supplied to the corresponding data lines for the enable period of an input source output enable signal, and a reference voltage of the liquid crystal cells is commonly supplied to the corresponding data lines for the disable period.

47. The method according to claim 35, further comprising raising a voltage of the time-divided pixel data after the performing a time-division on a digital pixel data.